WHAT IS CLAIMED IS:

1. A method of fabricating a capacitor electrode, comprising:

forming an etch stop layer over a surface of an interlayer insulating layer and over a surface of a conductive plug extending at a depth from the surface of the interlayer insulating layer;

forming a lower mold layer over the etch stop layer, and adjusting a wet etch rate of the lower mold layer by adding dopants to the lower mold layer during formation of the lower mold layer, and by annealing the lower mold layer;

forming an upper mold layer over the surface of the lower mold layer, wherein a wet etch rate of the upper mold layer is less than the adjusted wet etch rate of the lower mold layer;

dry etching the upper mold layer, the lower mold layer and the etch stop layer to form an opening therein which exposes at least a portion of the surface of the contact plug;

wet etching the upper mold layer and the lower mold layer so as to increase a size of the opening at the lower mold layer and so at to expose a surface portion of

the etch stop layer adjacent the surface of the conductive plug; and

depositing a conductive material over the surface of the opening in the upper and lower mold layers, the surface portion of the etch stop layer, and an exposed surface of the conductive plug.

2. The method of claim 1, further comprising removing the upper and lower mold layers after depositing the conductive material.

3. The method of claim 1, wherein the lower mold layer is formed of a doped oxide by chemical vapor deposition.

4. The method of claim 3, wherein the lower mold layer is formed of at least one of borophosphosilicate glass (BPSG) and phosphosilicate glass (PSG).

5. The method of claim 1, wherein the upper mold layer is formed of an undoped oxide by plasma enhanced chemical vapor deposition.

6. The method of claim 1, wherein the upper mold layer is formed of at least one of plasma-enhanced tetraethyllorthosilicate (PE-TEOS), high-density plasma (HDP) oxide, and P-SiH_4 oxide.

7. The method of claim 1, wherein the lower mold layer is formed of borophosphosilicate glass (BPSG), and wherein phosphorous and boron are added to the BPSG prior to said annealing.

8. The method of claim 7, wherein the boron is added in an amount of 2-3 wt% of the BPSG, and the phosphorous is added in an amount of 2-3 wt% of the BPSG.

9. The method of claim 1, wherein the lower mold layer is formed of phosphosilicate glass (PSG), and wherein phosphorous is added to the PSG prior to said annealing.

10. The method of claim 9, wherein the phosphorous is added in an amount of less than 5 wt% of the PSG.

11. The method of claim 1, further comprising cleaning a surface of the lower mold layer having the adjusted wet etch rate prior to forming the upper mold layer.

12. The method of claim 11, wherein H_2SO_4 is used to clean the surface of the lower mold layer.

13. The method of claim 1, wherein the conductive layer is deposited as a polysilicon by low pressure chemical vapor deposition.

14. The method of claim 1, wherein the upper mold layer and the lower mold layer are wet etch using at least one of SC1 (NH_4OH/H_2O_2/deionized water) and HF (hydrofluoric acid).

15. The method of claim 1, wherein the etch stop layer is silicon nitride, and the annealing of the lower mold layer is carried out at a temperature of less than

700°C.

16. The method of claim 1, wherein the conductive material forms a cylindrical electrode defined by a cylindrical wall and a bottom wall which extends over a surface of the conductive plug, wherein the cylindrical wall extends upwardly from the bottom wall away from the surface of the interlayer insulating layer;

wherein the cylindrical wall of the cylindrical electrode is defined by an upper cylindrical wall portion, a lower cylindrical wall portion, and an intermediate cylindrical wall portion located between the upper and lower cylindrical wall portions;

wherein a diameter of the upper cylindrical wall portion and a diameter of the lower cylindrical wall portion increase with an increase in a distance from the surface of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions decreases with an increase in a distance away from the surface of the bottom wall, and wherein

$$A \geq C, \quad C > B, \quad \text{and} \quad C > D$$

where A is a diameter of the upper cylindrical wall portion at a location farthest

from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a location farthest from the bottom wall, and D is a diameter of the lower cylindrical wall portion at the bottom wall.

17. A method of fabricating a capacitor, comprising forming a lower electrode over an interlayer insulating layer, forming a dielectric layer over the lower electrode, and forming an upper electrode over the dielectric layer, wherein said forming a lower electrode comprises:

forming an etch stop layer over a surface of the interlayer insulating layer and over a surface of a conductive plug extending at a depth from the surface of the interlayer insulating layer;

forming a lower mold layer over the etch stop layer, and adjusting a wet etch rate of the lower mold layer by adding dopants to the lower mold layer during formation of the lower mold layer, and by annealing the lower mold layer;

forming an upper mold layer over the surface of the lower mold layer, wherein

a wet etch rate of the upper mold layer is less than the adjusted wet etch rate of the lower mold layer;

dry etching the upper mold layer, the lower mold layer and the etch stop layer to form an opening therein which exposes at least a portion of the surface of the contact plug;

wet etching the upper mold layer and the lower mold layer so as to increase a size of the opening at the lower mold layer and so at to expose a surface portion of the etch stop layer adjacent the surface of the conductive plug; and

depositing a conductive material over the surface of the opening in the upper and lower mold layers, the surface portion of the etch stop layer, and an exposed surface of the conductive plug.

18. The method of claim 17, wherein said forming a lower electrode further comprises:

depositing an insulating layer over the conductive material and within the opening;

removing a portion of the insulating layer and the conductive material to expose the upper mold layer; and

removing a remaining portion of the insulating layer and the upper and lower mold layers.

19. The method of claim 17, wherein the lower mold layer is formed of a doped oxide by chemical vapor deposition.

20. The method of claim 17, wherein the lower mold layer is formed of at least one of borophosphosilicate glass (BPSG) and phosphosilicate glass (PSG).

21. The method of claim 17, wherein the upper mold layer is formed of an undoped oxide by plasma enhanced chemical vapor deposition.

22. The method of claim 17, wherein the upper mold layer is formed of at least one of plasma-enhanced tetraethyllorthosilicate (PE-TEOS), high-density

plasma (HDP) oxide, and P-SiH_4 oxide.

23. The method of claim 17, wherein the lower mold layer is formed of borophosphosilicate glass (BPSG), and wherein phosphorous and boron are added to the BPSG prior to said annealing.

24. The method of claim 23, wherein the boron is added in an amount of 2-3 wt% of the BPSG, and the phosphorous is added in an amount of 2-3 wt% of the BPSG.

25. The method of claim 17, wherein the lower mold layer is formed of phosphosilicate glass (PSG), and wherein phosphorous is added to the PSG prior to said annealing.

26. The method of claim 25, wherein the phosphorous is added in an amount of less than 5 wt% of the PSG.

27. The method of claim 17, further comprising cleaning a surface of the

lower mold layer having the adjusted wet etch rate prior to forming the upper mold layer.

28. The method of claim 27, wherein H_2SO_4 is used to clean the surface of the lower mold layer.

29. The method of claim 17, wherein the conductive layer is deposited as a polysilicon by low pressure chemical vapor deposition.

30. The method of claim 17, wherein the upper mold layer and the lower mold layer are wet etch using at least one of SC1 (NH_4OH/H_2O_2/deionized water) and HF (hydrofluoric acid).

31. The method of claim 17, wherein the etch stop layer is silicon nitride, and the annealing of the lower mold layer is carried out at a temperature of less than 700°C.

32. The method of claim 18, wherein the conductiv material forms a cylindrical lower electrode defined by a cylindrical wall and a bottom wall which extends over a surface of the conductive plug, wherein the cylindrical wall extends upwardly from the bottom wall away from the surface of the interlayer insulating layer;

wherein the cylindrical wall of the cylindrical lower electrode is defined by an upper cylindrical wall portion, a lower cylindrical wall portion, and an intermediate cylindrical wall portion located between the upper and lower cylindrical wall portions;

wherein a diameter of the upper cylindrical wall portion and a diameter of the lower cylindrical wall portion increase with an increase in a distance from the surface of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions decreases with an increase in a distance away from the surface of the bottom wall, and wherein

$$A \geq C, \quad C > B, \quad \text{and} \quad C > D$$

where A is a diameter of the upper cylindrical wall portion at a location farthest from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location

nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a location farthest from the bottom wall, and D is a diameter of the lower cylindrical wall portion at the bottom wall.

33. A capacitor comprising:

an interlayer insulating layer having a surface;

a conductive plug extending at a depth from the surface of the interlayer insulating layer;

an etch stop layer extending over the insulating layer and exposing the conductive plug;

a cylindrical lower electrode defined by a cylindrical wall and a bottom wall which extends over a surface of the conductive plug and over a portion of the etch stop layer adjacent the conductive plug, wherein the cylindrical wall extends upwardly from the bottom wall away from the surface of the interlayer insulating layer;

a dielectric layer formed over the cylindrical lower electrode; and

an upper electrode formed over the dielectric layer;

wherein the cylindrical wall of the cylindrical lower electrode is defined by an upper cylindrical wall portion, a lower cylindrical wall portion, and an intermediate cylindrical wall portion located between the upper and lower cylindrical wall portions;

wherein a diameter of the upper cylindrical wall portion and a diameter of the lower cylindrical wall portion increase with an increase in a distance from the surface of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions decreases with an increase in a distance away from the surface of the bottom wall, and wherein

$$A \geq C, \quad C > B, \quad \text{and} \quad C > D$$

where A is a diameter of the upper cylindrical wall portion at a location farthest from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a location farthest from the bottom wall, and D is a diameter of the lower cylindrical wall portion at the bottom wall.

34. The capacitor of claim 33, wherein the etch stop film is a silicon nitride film.

35. The capacitor of claim 33, wherein the lower electrode is a polysilicon electrode.

36. The capacitor of claim 33, wherein the dielectric layer is an oxynitride (NO) layer.